REMARKS

Claims 1-18 and 21-121 are pending in this application, with claims 1, 14, 16, 21, 25, 31, 39, 46, 59, 63, 69, 77, 84, 97, 101, 107 and 115 being independent. Claims 14-18 have been withdrawn from consideration, claims 19 and 20 have been canceled, and claims 21-121 have been added.

Initially, applicant thanks the Examiner for the interview granted on April 12, 2004. As discussed at the interview, at least three bases exist for distinguishing the subject matter of claim 1 from the cited prior art: that the metal line extends over the semiconductor layer, that the semiconductor layer is between the signal lines, or that the signal lines are metal.

Applicant also acknowledges with appreciation the Examiner's indication that claims 2-9 are directed to allowable subject matter.

Claim 1 has been amended to change the reference to a semiconductor "layer" to a semiconductor "island," to clarify the relationship between the signal lines and the semiconductor island, and to recite that the metal wiring line overlaps the crystalline semiconductor island. Support for this amendment may be found in Fig. 1C, which shows the metal wiring line 26 overlapping the crystalline semiconductor film 15, which is in the form of an island.

Claim 1 has been rejected as being anticipated by Yamazaki. Applicant requests reconsideration and withdrawal of this rejection because, as discussed at the interview, Yamazaki does not describe or suggest an arrangement in which a metal wiring line that connects two signal lines at least partially overlaps a semiconductor island that is also overlapped by the signal lines. The action equates the N-type impurity regions 126 and 127 with the first signal line and the second signal line. However, since those regions are not connected by a metal wiring line, they cannot constitute the two signal lines. Similarly, since the aluminum line 140 that connects the N-type impurity region 127 to the P-type impurity region 128 does not overlap with the gate electrode 104 that the Examiner has equated with the crystalline semiconductor island, the regions 127 and 128 also cannot constitute the two signal lines.

Like claim 1, each of new independent claims 21, 25 and 31 recites a metal wiring line that connects two signal lines and at least partially overlaps a semiconductor island that is also overlapped by the signal lines. All of these claims differ from claim 1 in that each of claims 21, 25 and 31 recites a semiconductor island, while claim 1 recites a crystalline semiconductor island. As discussed at the interview, recitation of a semiconductor island is believed to find support in the narrower recitation of a crystalline semiconductor island, as discussed above with respect to claim 1, since a crystalline semiconductor island is an example of a semiconductor island.

Claim 25 further differs from claim 1 in that claim 25 recites second and third circuits that each include a transistor and are connected, respectively, to the first and second signal lines. Support for this recitation may be found, for example, in Fig. 8A, which shows the first protective circuit 702 being connected between a driving circuit region and a pixel circuit region, each of which includes a transistor.

Claim 31 further differs from claim 1 in that claim 31 further recites a second circuit having properties similar to those of the first circuit, and third and fourth circuits that each include a transistor. Claim 31 also recites that the first signal line is connected to the third circuit and that the second signal line is connected to a signal line of the second circuit. Support for this recitation may be found, for example, in Fig. 8A, which shows the first protective circuit 802 being connected between a pixel region 801 and a second protective circuit 803.

Applicant requests allowance of claims 21, 25 and 31, along with their dependent claims, for the reasons discussed above with respect to claim 1.

Similarly to claim 1, claim 39 recites a metal wiring line that connects two signal lines that, respectively, partially overlap first and second semiconductor islands that are both partially overlapped by a third signal line. Support for this recitation may be found, for example, in Figs. 13A and 13B, which show a first signal line 1206, a second signal line 1208, a third signal line 1205, and a metal wiring line 1210. For reasons similar to those discussed above with respect to claim 1, Yamazaki does not describe or suggest an arrangement such as is recited in claim 39. Accordingly, applicant requests allowance of claim 39 and its dependent claims.

Independent claim 46 differs from claim 1 in that claim 46 recites that the first and second signal lines are metal signal lines, and does not recite that the metal wiring line overlaps the semiconductor island. Support for the recitation of metal signal lines may be found, for example, in Figs. 4A and 4B, which show that signal lines 308 and 309 are made from metal layers 302 and 303 (see page 20, lines 20-24). As discussed at the interview, Yamazaki's impurity regions 126-128, which the action equates to the signal lines, are made from silicon and, accordingly, cannot constitute the recited metal wiring lines. Accordingly, for at least this reason, applicant requests allowance of claim 46 and its dependent claims.

Independent claims 59, 63, 69 and 77 are similar to claims 21, 25, 31 and 39 respectively, and differ from those claims in the same way that claim 46 differs from 1. In particular, each of claims 59, 63, 69 and 77 recites metal signal lines. Accordingly, applicant requests allowance of claim 59, 63, 69 and 77, along with their dependent claims, for the reasons discussed above with respect to claim 46.

Independent claim 84 differs from claim 1 in that claim 84 recites that the semiconductor island is interposed between the first and second signal lines, and does not recite that the metal wiring line overlaps the semiconductor island. Support for the recitation of having the semiconductor island interposed between the signal lines may be found, for example, in Fig. 1A, which shows the semiconductor island 15 interposed between the signal lines 18 and 19. As discussed at the interview, Yamazaki's impurity regions 127 and 128, which are connected by a metal wiring line, cannot be said to correspond to the recited signal lines because the semiconductor island is not interposed between them. Similarly, the regions 126 and 127 cannot be said to correspond to the recited signal lines because they are not connected by a metal wiring line. Accordingly, for at least this reason, applicant requests allowance of claim 84 and its dependent claims.

Independent claims 97, 101, 107 and 115 are similar to claims 21, 25, 31 and 39 respectively, and differ from those claims in the same way that claim 84 differs from 1. In particular, each of claims 97, 101, 107 and 115 recites a semiconductor island interposed

between the signal lines. Accordingly, applicant requests allowance of claim 97, 101, 107 and 115, along with their dependent claims, for the reasons discussed above with respect to claim 84.

Applicant submits that all claims are in condition for allowance.

Enclosed is a check for $3,918 ($2,728 for excess claims fees, $770 for Request for Continuation of Examination fee and $420 for the Petition for Extension of Time fee). Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

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